

課題番号 : F-21-UT-0154  
利用形態 : 機器利用  
利用課題名(日本語) : 単一分子薄膜-細胞の電極準備  
Program Title (English) : Single Molecular-Single cell electrode preparation  
利用者名(日本語) : リ シェオ、金秀炫  
Username (English) : LI Shuo, Kim Soo Hyeon  
所属名(日本語) : 東京大学生産技術研究所  
Affiliation (English) : Institute of Industrial Science, The University of Tokyo  
キーワード/Keyword : リソグラフィ・露光、成膜・膜堆積、膜加工、熱処理、表面処理、切削

## 1. 概要(Summary)

Gold surface and gold nanodots are fabricated on silicon chips by using e-beam lithography and sputtering. In addition, holes and trench pattern on Si are fabricated by using DRIE.

## 2. 実験(Experimental)

### 【利用した主な装置】

超高速大面積電子線描画装置  
4 インチ高真空 EB 蒸着装置  
LL 式高密度汎用スパッタリング装置  
レーザー直接描画装置  
高速シリコン深掘りエッチング装置

### 【実験方法】

E-beam lithography and metallization processes were used here. The details of the process are shown as below;

#### i. Cleaning

The substrate is cleaned by sonication in a bath of acetone and ethanol for 5 min, respectively, then dried with blowing nitrogen at room temperature.

#### ii. Resist spin coating

ZEP and JSR resists are used for E-beam and Laser writing, respectively.

#### iii. E-beam exposure or Laser exposure

#### iv. Development

After e-beam or laser writing, the sample is put in the right developer for appropriate time and followed with rinsing under flowing DI water and dried with nitrogen.

#### v. Metallization

The gold electrodes are deposited by using

Sputter CFS-4EP-LL i-Miller.

## 3. 結果と考察(Results and Discussion)

Fig. 1(a) shows the scanning electron microscope (SEM) image of the gold nanodots, the height of the nanodot is 10 nm. Fig. 1(b), (c) present the photo of the silicon chip with through holes and trench pattern that fabricated by DRIE.

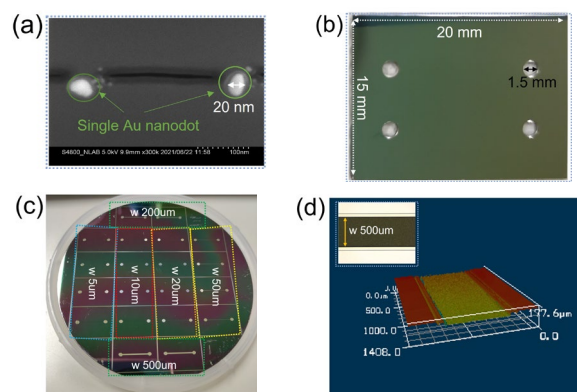


Fig. 1(a) SEM image of the nanodots sample, (b) image of the Au/Si chip with desired dimension of through holes, (c) image of trench pattern on Si wafer (trench dimension, W: Width, Length: 14.5 mm), (d) 3D laser microscopy image to show the trench (width: 500 μm, height: 13.8 μm)

## 4. その他・特記事項(Others)

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## 5. 論文・学会発表(Publication/Presentation)

なし

## 6. 関連特許(Patent)

A patent has been submitted.