課題番号 :F-20-WS-0088
利用形態 :機器利用
利用課題名(日本語) :高温で低いサブスレッショルドスイングを実現する C-Si ダイヤモンド MOSFET
Program Title (English) :C-Si Diamond MOSFET achieving low subthreshold swing at high temperature
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キーワード／Keyword : ICP-RIE エッチング、電気計測.

1. 概要(Summary)

A C-Si diamond MOSFET is fabricated at a diamond/SiO_2 interface through MPCVD at a high temperature of over 800 °C. This is different from the thermal oxidation treatment in Silicon technology. In this work, in order to achieve a high performance C-Si diamond MOSFET, nanotechnology research center (NTRC) of Waseda University has been utilized to fabricate and measure the C-Si diamond devices.

2. 実験(Experimental)

【利用した主な装置】

クリーンルーム、両面マスクアライナ、ICP-RIE 装置、プラズマ処理装置、プラズマリアクター、FE-SEM (S-4800)、高耐圧デバイス測定装置。

【実験方法】

(1) The undoped diamond layer and the SiO_2 film deposition on the (100) diamond substrate.
(2) The source/drain diamond selective growth region etching.
(3) The boron doped diamond selective growth (C-Si bonds formation process) via MPCVD.
(4) Ohmic electrodes deposition by EB system.
(5) The isolation via ICP-RIE and oxygen plasma.
(6) A 50 nm TEOS SiO_2 layer was deposition.
(7) An overlapping gate formation with 100 nm Al.

3. 結果と考察(Results and Discussion)

Fig. 1 shows (a) the schematic diagram (b) the opticalmicroscope picture of the device, which contains TEOS SiO_2 selective growth mask and passivation layer. Fig. 2 shows the Current-Voltage performances of the device with high current and low subthreshold swing *(SS)* at high temperature. The *SS* of a device is defined as the change in gate voltage which must be applied in order to create a one decade increase in the output current. The low *SS* value (250 mV/dec @150 nm SiO_2 gate oxide) permits a lower threshold voltage for the same off-current, which in turn allows the device to be used at lower supply voltages thereby attracting attention for low power operation. In a word, the result of this work promotes the integration of Si process with diamond material.

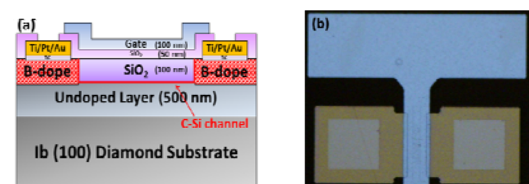

Fig. 1 (a) The schematic diagram and (b) opticalmicroscope picture of the C-Si device.

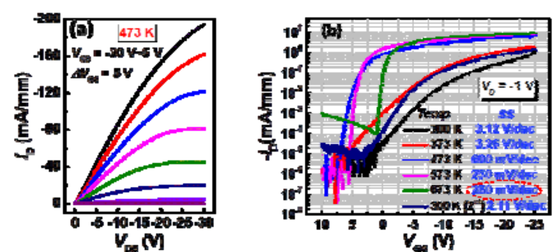

Fig. 2 (a) The I_D-V_{DS} Characteristics of the fabricated device at 473 K, and (b) the I_D-V_{GS} Characteristics at different temperature.

4. その他・特記事項(Others)

・関連文献

(1) T. Bi, Y. Chang, W. Fei, M. Iwataki, A.

Morishita, **Y. Fu**, N. Niikura, and H. Kawarada,
Carbon. 175 (2021) 525-533.

5. 論文・学会発表（Publication/Presentation）

なし。

6. 関連特許（Patent

なし。