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利用形態　　:機器利用
利用課題名（日本語）　:ナノフルイディクスのためのナノ・マイクロチャネル製作
Program Title (English)　:Micro and nanochannels fabrication for nanofluidics
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キーワード／Keyword　:リソグラフィ・露光・描画装置，バイオ&ライフサイエンス，ナノフルイディクス

1．概要（Summary）

Transport of fluids and ions confined at the nanoscale strongly deviates from the continuum description of classical hydrodynamics. Nanofluidics consists in the study of these exotic transport properties which take their roots in the combination, at the nanoscale, of the richness of the surface-driven physical phenomenon such as charge effects, fluctuations or fluid slippage. To this end we fabricate by a top-down approach micro and nano channels in a quartz wafer.

2．実験（Experimental）

【利用した主な装置】

レーザー直接描画装置, LL 式高密度汎用スパッタリング装置, 汎用平行平板 RIE 装置, 汎用 ICP エッチング装置, クリーンドラフト潤沢超純水付, 形状・膜厚・電気特性評価装置群, ニッケルめっき装置

【実験方法】

In this study, we are developing a process using direct laser lithography to etch in quartz a channel network combining nanometric channels (nanometric depth, micrometric width and length) supplied in liquid by micrometric channels (Fig. 1a).

First, using direct laser writing (DWL66+) of JSR7790G resist, we create a mask quartz etching with a nanometric depth (400 nm). Etching is performed using either Samco RIE-10NR or ICP-RIE ULVAC CE-300I.

The second step consist of microchannels etching with a typical depth of 50 µm. To do so, we first deposit with Shibaura CFS-4EP-LL, a seed layer of Cr/Au (5/100 nm) for later electroplating. Using DWL66+, the microchannels design is transferred to AZ P4620 photoresist (we use alignment marks for proper continuity between micro and nanochannels). After development, the gold layer is used for Nickel electroplating, we obtain a micrometric nickel layer for later etching.

3．結果と考察（Results and Discussion）

With the previous process, we managed to etch nanochannels (Fig. 1c), and we are currently developing the last part of the process for deep etching of the microchannels with Ni mask. Due to the poor thermal conductivity of glass, temperature can be much higher when etching glass compared with equivalent silicon etching. This can cause damage to the resist and eventually to the etching machine. Therefore, extra care should be paid to temperature management during the processes.

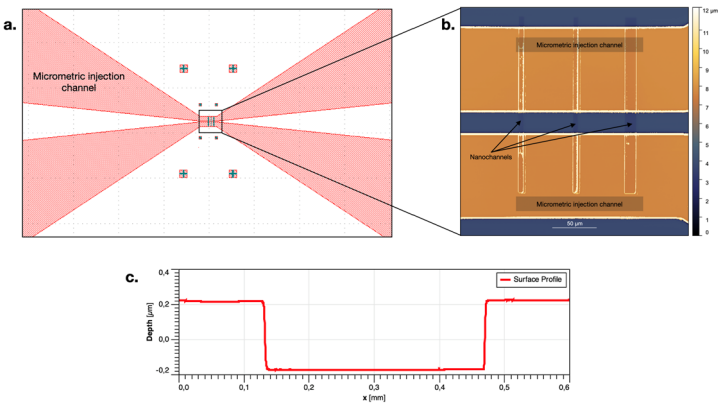

Fig. 1 Micro/nano channels system. **a.** Two layers lithography schematics. **b.** Height map of the AZ P4620 photoresist for Ni electroplating before microchannels etching. **c.** Dektak profile of one nanochannel etched in glass. Depth = 400 nm.

4. その他・特記事項（Others）

We would like to thank 水島彩子 and Eric Lebrasseur（東京大学）for their support with the process and operating DWL66+, Ni electroplating and ICP-RIE ULVAC CE-300I.

5. 論文・学会発表（Publication/Presentation）

なし

6. 関連特許（Patent）

なし