

課題番号 : F-20-UT-0071
利用形態 : 機器利用
利用課題名(日本語) : 単一分子薄膜電極準備
Program Title (English) : Single Molecular electrode preparation
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キーワード/Keyword : リソグラフィ・露光・描画装置、成膜・膜堆積、膜加工・エッチング、熱処理、表面処理

1. 概要(Summary)

Gold surface and gold nanodot arrays are fabricated on silicon chips by using e-beam lithography. In addition, holes on Si chip are fabricated by using DRIE. In the end, an attempt will be made to graft a single aptamer molecule per nanodot as biosensor platform and microfluidic channels will be formed with these chip holes.

2. 実験(Experimental)

【利用した主な装置】

超高速大面積電子線描画装置
4 インチ高真空 EB 蒸着装置
LL 式高密度汎用スパッタリング装置
レーザー直接描画装置
高速シリコン深掘りエッチング装置

【実験方法】

E-beam lithography and metallization processes were used here. The details of the process are shown as below:

- i. Cleaning
The substrate is cleaned by sonication in a bath of acetone and ethanol for 5min, respectively, and then dried with blowing nitrogen at room temperature.
- ii. Resist spin coating
ZEP and JSR resists are used for E-beam and Laser writing, respectively.
- iii. E-beam exposure or Laser exposure
- iv. Development
After e-beam or laser writing, the sample is put in the right developer for appropriate

time and followed with rinsing under flowing DI water and dried with nitrogen.

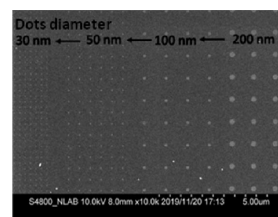
v. Metallization

The gold electrodes are deposited by using ultra high vacuum evaporator NSP2 or Sputter CFS-4EP-LL i-Miller.

3. 結果と考察(Results and Discussion)

Figure 1(a) shows the scanning electron microscope (SEM) image of the gold nanodots with different diameters, the height of the nanodot is around 10 nm. Figure 1(b) presents the photo of the 2 cm x 2 cm silicon chip with through holes that fabricated by DRIE.

(a)



(b)

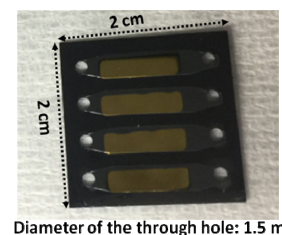


Figure 1(a). SEM image of the nanodots sample, (b) image of the Silicon chip with desired dimension of through holes.

4. その他・特記事項(Others)

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5. 論文・学会発表(Publication/Presentation)

なし

6. 関連特許(Patent)

なし