課題番号　　:F-20-AT-0143
利用形態　　:機器利用
利用課題名（日本語）　　:pMOS デバイスのゲート酸化物としての酸化ケイ素
Program Title(English)　　:Silicon oxide as gate oxide for pMOS devices
利用者名（日本語）　　:ロザック　ミカエル
Username(English)　　:Mickael Lozac'h
所属名（日本語）　　:一般社団法人ミニマルファブ推進機構、 産業技術総合研究所
Affiliation(English)　　:Minimal Fab Promoting Organization, National institute of advanced industrial science and technology (AIST)
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1. 概要（Summary）

Our research focus on the silicon-oxide (Si-O) stretching mode from FTIR to assess the quality of p-channel metal-oxide-semiconductor field effect transistor (p-MOSFET), also called pMOS. We are investigating the possibility to link the density of interface states (D_{it}), between the gate oxide (SiO_x) and the Si wafer, and the Si-O stretching mode. Here, the optical properties of the silicon oxide are monitored by Fourier Transform Infra-Red (FTIR) and coupled with the gate oxide process, the chemical cleaning process prior to the gate oxide deposition, and D_{it} measured on pMOS devices.

2. 実験（Experimental）

【利用した主な装置】顕微フーリエ変換赤外分光装置 (FT-IR) 【実験方法】The pMOS devices are fabricated by Minimal Fab: an advanced, cost-effective, semiconductor fab where the area of the required cleanroom level is minimized to the surrounding of the silicon wafers (with a diameter of 12.5 mm), encapsulated in a shuttle during the full fabrication process. Then, the D_{it} estimated from C-V analysis and the Si-O stretching mode are systematically monitored.

3. 結果と考察（Results and Discussion）

For two pMOS devices A and B realized in a similar process, the D_{it} is estimated by C-V measurements at 5.5±1.0 $\times 10^{10}$ eV^{-1} cm^{-2} and 4.5±1.5 $\times 10^{11}$ eV^{-1} cm^{-2}, respectively. The Si-O stretching mode, located at the wavenumbers from 1000 cm^{-1} to 1250 cm^{-1}, and its deconvolution, is shown in Fig. 1. The devices are well deconvoluted into two peaks noted in-phase and out-of-phase (Fig. 1). Interestingly, the integrated area of the Si-O stretching out-of-phase is slightly larger for the pMOS device B that also presents a larger D_{it}. This could be attributed to some impurities present at the interface and/or some slight damages due to the fabrication process after the high temperature annealing (1150 °C for 1h) for the gate oxide. The nature of such impurity and its concentration or the possible process damages are still under investigation. Besides, the stoichiometry x of the silicon oxide (SiO_x) can also be determined with the position of the Si-O stretching mode in-phase. We estimate a similar stoichiometry about 1.91±0.01 and 1.92±0.01 for the pMOS devices A and B, respectively. Thus, coupling the FTIR analysis with D_{it} could be useful for the determination of the Gate oxide quality and its interface with the Si wafer.

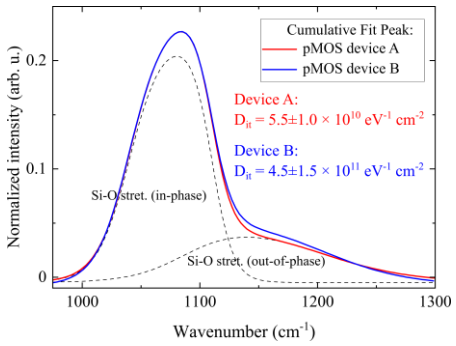

Fig. 1 FTIR Si-O stretching mode for two different pMOS devices A and B with respective D_{it}.

4. その他・特記事項（Others）

なし。

5. 論文・学会発表（Publication/Presentation）

(1) M. Lozac'h, S. Khumpuang, and S. Hara, JSAP 68th Spring Meeting (2021).

6. 関連特許（Patent）

なし。