

課題番号 : F-19-TU-0030
 利用形態 : 機器利用
 利用課題名(日本語) : MEMS/NEMS fabrication
 Program Title (English) : MEMS/NEMS fabrication
 利用者名(日本語) : Nguyen Van Toan
 Username (English) : Nguyen Van Toan
 所属名(日本語) : 東北大学大学院工学研究科
 Affiliation (English) : Graduate School of Engineering, Tohoku University
 キーワード/Keyword : 膜加工・エッチング, Nanoelectromechanical switches, logical gates, NAND, NOR

1. 概要(Summary)

This work focuses on the design, fabrication and evaluation of electrostatically driven nano electromechanical switches and logical gates including NAND and NOR gates. Conformal deposition of tungsten on high aspect ratio structures is investigated by selective W chemical vapor deposition as an electrical contact material. Logical gates including NAND and NOR gates are formed by four the NEM switches consisted of four cantilevers, two input ports, two source ports, and output.

2. 実験(Experimental)

【利用した主な装置】

- . W-CVD 装置
- . Vapor HF エッチング装置
- . エッチングチャンバー
- . DeepRIE 装置#1
- . メタル拡散炉
- . サンドブラスト
- . 両面アライナ露光装置一式(両面アライナ、スピスコータ、オーブン、現像機、乾燥機)

【実験方法】

Devices are fabricated using SOI wafers. To save the exposing time of electron beam lithography process, a combination between electron beam lithography and standard lithography is proposed. Electron beam lithography creates nano-gaps while standard lithography produces large areas.

Devices are successfully fabricated by a combination of an electron beam lithography, a deep reactive ion etching, and a selective W chemical vapor deposition. Truth table operations of NAND and NOR are examined and demonstrated.

3. 結果と考察(Results and Discussion)

Fig. 1 shows the Tungsten can be uniformly deposited on the high aspect ratio of silicon trenches successfully. Fig. 2 demonstrates the individual nanoelectromechanical switch.

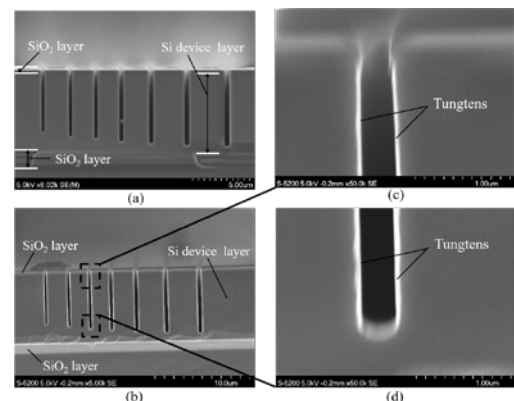


Fig. 1. Testing sample on selective Tungstens deposition.

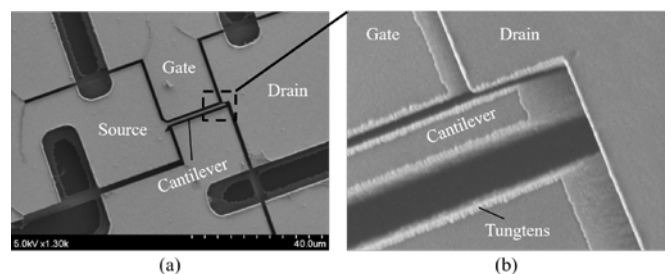


Fig. 2. Individual nanoelectromechanical switch.

4. 論文・学会発表(Publication/Presentation)

1. N.V. Toan, D. Zhao, N. Inomata, M. Toda, Y. Song, and T. Ono, "Design and fabrication of electrostatically driven nanoelectromechanical logical gates", *Phys. Status Solidi A* **216**, 1800797, 2019.

5. 論文・学会発表(Publication/Presentation)

なし

6. 関連特許(Patent)

なし