課題番号　:F-19-OS-0057
利用形態　:機器利用
利用課題名（日本語）　:高電流密度下での Sn-Ag はんだのエレクトロマイグレーション現象
Program Title (English)　:Electromigration in Sn-Ag solder thin films under high current density
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キーワード／Keyword　:Thin film, reliability, electromigration, 成膜・膜堆積

1. 概要（Summary）

The electro-migration (EM) behavior of a Sn–Ag solder thin film stripe that is deposited on a glass substrate has been investigated under a high current density in the absence of thermo-migration. The distribution of voids and hillocks at current densities of 4.4–6.0 × 10^4 A/cm^2 has been analyzed optically and using electron microscopy. The voids mainly formed at the cathode side of the stripe where maximum current density was predicted but voids also formed along a line that crosses the stripe. This was explained in terms of the initial voids forming at locations of maximum current density concentration, altering these locations, and then expanding into them. The movement of the maximum current density location is caused by redistribution of current as the voids form. However, the temperature dependence of the diffusivity of atoms is sufficient to account for void nucleation within the timescale of the experiments.

2. 実験（Experimental）

【利用した主な装置】

EB 蒸着装置（Model: UEP-2000 OT-H/C）

【実験方法】

A Cr adhesion film with 5 ± 1 nm thickness is coated on a 150 μm thick glass cover slip using an evaporation technique in vacuum. A nominally 305 ± 5 nm thick Sn is deposited on top of the Cr using the same technique. The 305 μm wide, 5 mm long solder stripe geometry was created by using a glass mask during the evaporation deposition process.

3. 結果と考察（Results and Discussion）

Without EM test, particles deposited on the glass homogenously and no void could be observed on the stripe as shown on the Fig. 1. After EM for 120 h, some voids could be observed on the cathode side, this phenomenon was different comparing with the results observed on the Cu or Al connected solder joint which proposed that it took 88% of the failure time to initiate the few voids, whereas only 12% of the failure time was spent in void propagation until the final open failure.

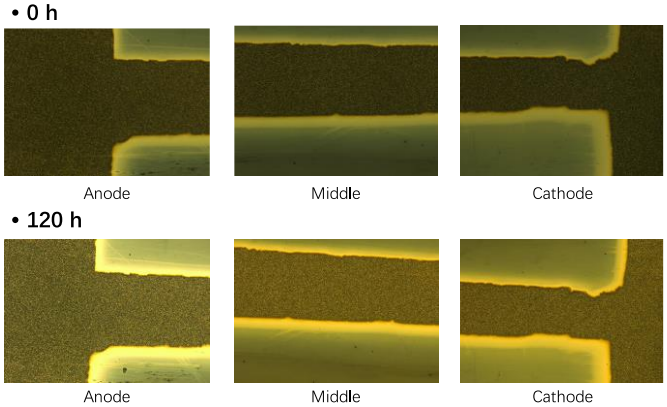

Fig. 1. The morphology change of the sample after EM test

4. その他・特記事項（Others）

参考文献:[1] Chan, Y. C., & Yang, D. (2010). Failure mechanisms of solder interconnects under current stressing in advanced electronic packages. Progress in Materials Science, 55(5), 428-475.

5. 論文・学会発表（Publication/Presentation）

Zhi Jin, Yu-An Shen, Fupeng Huo, Y.C. Chan, Hiroshi Nishikawa, *Journal of materials science*, accepted.

6. 関連特許（Patent）

なし