課題番号　:F-19-KT-0107
利用形態　:機器利用
利用課題名（日本語）　:(100)単結晶シリコンを用いた同調型振動リングジャイロスコープにおける形状補償
Program Title(English)　:Geometrical Compensation for Mode-Matching of (100) Silicon Ring Resonator for Vibratory Gyroscope
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キーワード／Keyword　:単結晶シリコン、ジャイロスコープ、膜加工・エッチング

1. 概要（Summary）

A vibratory ring gyroscope (VRG) with non-uniform radial width to compensate the elastic anisotropy of (100) SCS was introduced and characterized by the finite element analysis (FEA) simulation and experiments [1]. Moreover, the effect of suspending beams of a VRG on Δf was also analyzed and their dimensions were optimized to achieve minimal Δf of 9Hz in simulation which was nearly mode-matched. With this proposed geometrical compensation, a VRG was fabricated by standard SOI fabrication process using a (100) SCS wafer with a 22-μm-thick device layer. In the frequency response test, the compensated VRG shown a smaller Δf, 126 Hz, than the uncompensated one with uninform radial width, 189 Hz.

2. 実験（Experimental）

【利用した主な装置】

[A03] Laser Pattern Generator, [A05] High Precision Double-Sided Mask Aligner, [B08-1] Deep Reactive Ion Etching machine

【実験方法】

The compensated and uncompensated VRGs were both fabricated on (100) silicon-on insulator (SOI) wafers of a 22-μm-thick device layer. Firstly, the ring and suspending beams were patterned using ultraviolet (UV) lithography (Mask aligner, MA6 BSA, SUSS MicroTec) and deep reactive-ion etching (DRIE) (RIE-800iPB-KU, Samco). After photoresist removal, the 7-μm-thick negative photoresist (PMER P-WG300, Tokyo Ohka Kogyo) was spin-coated and electrode pads were patterned by UV lithography (Mask aligner, PEM-800, Union Optical). Then the aluminum layer of 200 nm thickness was deposited by electron beam deposition (EB1200, Canon). And Lift off process with n-methyl-2-pyrrolidone (NMP) was used to pattern the aluminum electrode pads. Finally, the 2-μm-thick sacrificial layer was etched by vapor hydrofluoric acid (MLT-SLE-0x, Sumitomo Precision Products) and the structures of ring and suspending beams were released.

3. 結果と考察（Results and Discussion）

A fabricated device chip is also shown in Fig. 1.

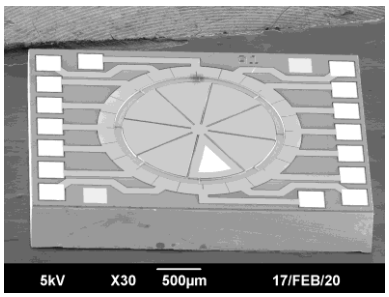

Fig. 1 Device image of a VRG.

4. その他・特記事項（Others）

・参考文献

[1] Hopcroft M. A. et al., J. Microelectromech. Syst., 2010, 19(2): 229-238.

5. 論文・学会発表（Publication/Presentation）

(1) S. Yunyi, Y. Hirai, and T. Tsuchiya. The 7th IEEE International Symposium on Inertial Sensor & Systems (INERTIAL 2020), Hiroshima, Japan

6. 関連特許（Patent）　なし