課題番号 :F-18-AT-0120
利用形態 :機器利用
利用課題名(日本語) :
Program Title (English) :Design and Fabrication of Microneedle Pad
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Keyword :膜加工・エッチング, Patterning, microlens, Silicon etching

1. 概要(Summary)

In this project, we focus on the microneedle fabricated from photocurable resin/polymer. By utilizing optics such as microlens, UV light is focused into resin/polymer reservoir to form 'cone shape' microneedles. Hence, we aim to fabricate silicon holder for the microlens (see Figure 1). The back side of which will be use to hold the microlens while the front side is designed to locate a mask pattern to control the microneedle profile. The challenge of this project lies on how to align the back side hole and the front side pattern to obtain well-aligned light pathway for microneedle fabrication. Here, we propose the method which performing the back side anisotropic etching prior to the front side pattern etching to simplify the alignment process.

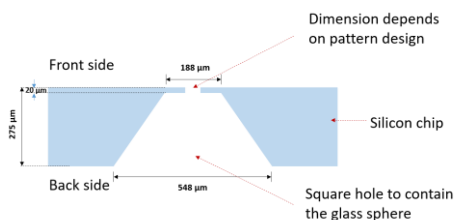

Figure 1: Schematic of the microlens holder.

2. 実験(Experimental)

【利用した主な装置】Major equipment used

スピンコーター, マスクレス露光装置, 多目的エッチング装置(ICP-RIE), 反応性イオンエッチング装置 (RIE), 電界放出形走査電子顕微鏡(S4800), 短波長レーザー顕微鏡[OLS-4100].

【実験方法】Experimental method

1.) Preparation of the back side pattern: 1 μm thermal oxide pre-coated silicon wafer was used in the process. First, Square pattern was transfer by photolithography technique onto PMER-HA 1300 PM photoresist (spin coating; 1250 rpm for 30 s, pre-baked 110°C for 10 min) on the back side of the 1 μm thermal oxide pre-coated silicon wafer. Subsequently, the film was developed twice by PMER P-7G for 3 min then post-baked at 110°C for 6 min.

2.) Etching of the square hole on the back side: Thermal oxide layer was removed by RIE (O_2:CF_4 17:54 sccm for 30 min) and was subsequently anisotropic etched by TMAH solution (90°C for 6.5 h) and washed in DI water.

3.) Preparation of the front side pattern: Circle array pattern was transfered on the PMER-HA 1300 PM photoresist layer of the front side using photolithography method (same photoresist preparation condition as step 1). Since, it is very important to align the patterns of both side, we optimized the back side etching to obtain a thin translucent film to assist the aligning step. The wafer was developed and post-baked using the same condition as step 1.

4.) Etching of the front side pattern: The front side thermal oxide layer was removed by ICP-RIE technique (CHF_3 50 sccm, pressure 1 Pa, ICP power 200 W, bias 150 W, 30 minutes). Then, the silicon was further removed using Bosch process

(Alternating between [step1] SF_6:Ar 50:20 sccm, ICP power 480 W, bias 25 W and [step2] CHF_3 70 sccmp, ICP power 400 W, bias 0 W for 50 cycles). After etching, surface of the wafer was cleaned by plasma asher equipment (300 W) for 40 minutes. The wafer was then characterized and cut into pieces.

3. 結果と考察(Results and Discussion)

The front side pattern (Figure 2) after the Bosch process showed circle with the diameter of 156 μm with the distance of 1012 μm between the patterns. When observe by SEM, it was found that the translucent layer composes of 2 layers, the SiO_2 top layer (0.9 μm) and the silicon bottom layer (7 μm). Thickness of this layer can be tuned by changing the back side wet etching time to optimize the strength and the translucent properties of the membrane. In addition, we observed the alignment of the front-back side pattern and found that both side pattern align well as shown in Figure 3.

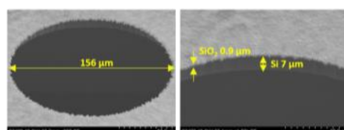

Figure 2: (left) SEM image of the front side circle pattern after the Bosch process, (right) SEM image showing SiO_2 and silicon layer.

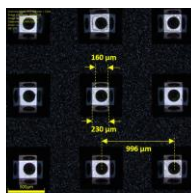

Figure 3: 3D OM image taken from the back side of the wafer showing the alignment between the front and back side pattern.

4. その他・特記事項(Others)

None.

5. 論文・学会発表(Publication/Presentation)

None.

6. 関連特許(Patent)

None.