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Program Title (English) : Design and Fabrication of Microneedle Pad
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1. 概要(Summary)

To obtain microneedle pad, microneedle master mold from silicon was designed and fabricated at NPF, AIST. Various patterns were used to study the fabrication process including simple shapes such as circle and square. Fabrication process started from producing the pattern hard mask of silicon dioxide which was pre-deposited onto silicon substrate. This hard mask was etched using ICP-RIE technique. The etching conditions were optimized to uncover silicon surface with minimum damage to the mask. After obtaining the hard mask, the samples were further etched by ICP-RIE technique to observe etching profile and etching rate.

2. 実験(Experimental)

【利用した主な装置】マスクレス露光装置,電界放出形走査電子顕微鏡(S4800), プラズマ CVD 装置(TEOS_SiO_2),スピンコーター,短波長レーザー顕微鏡[OLS-4100],多目的エッチング装置(ICP-RIE)

【実験方法】The fabrication process is as followings.

1) Thermal silicon dioxide with the thickness of 0.65 μm was deposited on the 6-inch silicon wafer.

2) An extra layer of silicon dioxide with the thickness of 4.35 μm was deposited on top of the thermal silicon dioxide using the plasma-enhanced chemical vapor deposition technique. This is to make the silicon dioxide hard mask thick enough for silicon deep etching.

3) In this step, thick photoresists were deposited on the silicon dioxide layer before the photolithography was performed to create pattern for silicon dioxide hard mask fabrication. The photoresist needs to be thick enough to protect the silicon dioxide from being etched until the hard mask was successfully fabricated. Two polymers were used as the photoresist;

A) Photoresist AZ5214E with the thickness of around 3 μm was deposited onto the PECVD silicon dioxide layer. First, the substrate was baked at 110 C for 1 min, then soaked in HMDS vapor for 1 min. Photoresist AZ5214E was spin coated by ramping from 0 to 1000 rpm in 10 s and continue at 1000 rpm for 30 s before ramping down to 0 rpm in 5 s. After the deposition, the photoresist was pre-baked at 90 C for 90 s, then photolithography process was performed to obtain the designed patterns i.e. circle or square array. The samples were subsequently developed in NMD-3 3.28% for 1 min before the reaction was stopped in water for 1 min. Finally, the samples were post-baked at 120 C for 4 min.

B) Photoresist PMER HA-1300 PM with the thickness of around 44 μm was deposited onto the PECVD silicon dioxide. Before the spin coating step, the substrates were prepared by the same procedure as 3)-A except that the substrates were not soaked in HMDS. The PMER HA-1300 PM was then spin coated by ramping from 0 to 2000 rpm in 10 s then kept at 2000 rpm for 30 rpm before ramping down to 0 rpm in 5 s. After the coating step, the photoresist pre-baked at 110 C for 6 min before the photolithography step. After that, the samples were developed in PMER P7G for 6 min and subsequently in water for 1-2 min. The samples were post-baked at 110 C for 15 min.

4) Inductively coupled plasma-reactive ion etching (ICP-RIE) technique was carried out to etch the silicon dioxide layer using condition as follow; pressure at 1 Pa, CHF_3 flow at 50 sccm, ICP power at 200 W, bias power at 150 W, and stage temperature at 20 C. The etching times were varied and the depths were measured to find the silicon dioxide etching rate.

5) After etching the silicon dioxide layer, the exposed silicon was further etched by the ICP-RIE using the following condition [1]; pressure at 4 Pa, flow of SF_6:O_2:Ar at 85:65:60 sccm, ICP power at 700 W, bias power at 30 W, and stage temperature at 20 C. Similar to the silicon dioxide layer etching, different etching time were performed to evaluate the silicon etching rate.

3. 結果と考察(Results and Discussion)

1) Silicon dioxide etching rate was evaluated on the AZ5214E sample. It was found that by using the etching condition as explained in the experimental 4), the silicon dioxide layer was completely removed within 50 min as shown in Figure 1. At this point, the silicon dioxide hard mask was obtained. The calculated etching rate was around 100 nm/min.

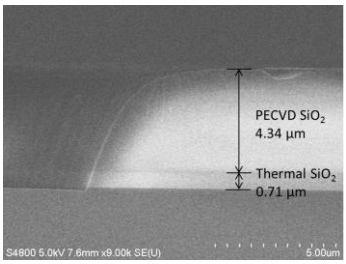

Figure 1: SEM image showing that the silicon dioxide was removed and the silicon surface was ready for further silicon etching step.

The results also suggest that using PMER HA-1300 PM can provide the hard mask for further silicon etching step as seen in Figure 2. However, it is noted that for a very small pattern size i.e. circle pattern with diameter of 14 µm, the hard mask cannot be achieved due to the too high aspect ratio between the pattern size to the resist thickness (14 µm : 44 µm).

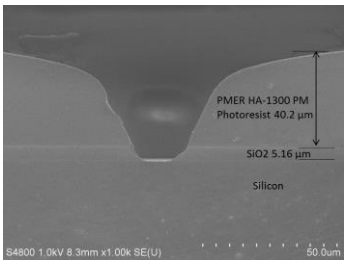

Figure 2: SEM image of the silicon dioxide hard mask fabricated by using PMER HA-1300 PM photoresist.

2) In the silicon etching step, it is clearly seen that the pattern size plays an important role on the silicon etching rate as shown in Figure 3. The pattern size of 20 µm (circle shape) yields the rate of 1.99 µm/min while the pattern size of 70 µm (square shape) results in 2.78 µm/min. the larger pattern tends to provide faster silicon etching rate even though the same etching condition was used.

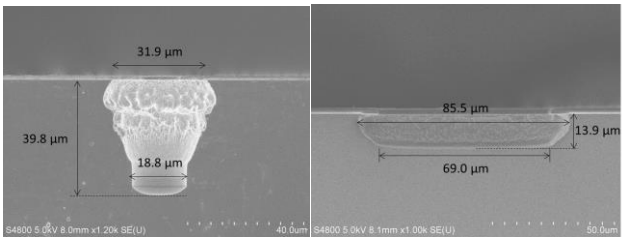

Figure 3: (Left) Cross sectional SEM image of the sample using 20 µm diameter circle pattern. After 20 min etching, the silicon depth is 39.8 µm. (Right) Cross sectional SEM image of the sample using 70 µm square pattern. Over 5 min silicon etching, the silicon depth is 13.9 µm.

In addition to the etching rate, the results in both cases also showed that the etching profile is taper shape which is important for fabricating silicon mold for microneedle. However, the results shown here are only from preliminary studies. Further studies are needed as it can be seen that experimental conditions depend on the require depth and the pattern size/shape.

4. その他・特記事項(Others)

[1] P. Dixit, *et al*, ECS Journal of Solid State Science and Technology, 1 (3) P107-P116, 2012

5. 論文・学会発表(Publication/Presentation) なし。

6. 関連特許(Patent) なし。