課題番号　　　　　　　　：F-15-IT-0008
利用形態　　　　　　　　：共同研究
利用課題名（日本語）　　：
Program Title (English)　：InAs Quantum Well MOSFETs Performance Improvement by Using pre-AlN Passivation Layer and In-Situ PEALD Post Remote Plasma Treatment

利用者名（日本語）　　　：張翼
Username (English)　　　：Edward Yi Chang
所属名（日本語）　　　　：国立交通大学　材料工学科，台湾
Affiliation (English)　　：Department of Materials Science and Engineering,
National Chiao Tung University, Taiwan

1. 概要（Summary）

This study demonstrates HfO_2 on InAs QW-MOSFETs with an AlN interfacial passivation layers. The device shows very good electrical characteristics, including low leakage current, subthreshold swing of 90 (mV/dec.) and DIBL of 80(mV/V).

2. 実験（Experimental）

【利用した主な装置】

electron beam exposure system, Electron-Beam Lithography Software

【実験方法】

The process for the InAs QW-MOSFETs including mesa isolation, e-beam lithography (EBL), the device cap layer removed in the EBL defined area, high-*k* gate dielectrics deposition and post deposition annealing, definition of contacts area and the removal of dielectrics, Metallization of S/D contacts and pads, Gate definition by EBL, and Gate metallization. The cross-section of photoresists for cap recess step was shown in Fig. 1.

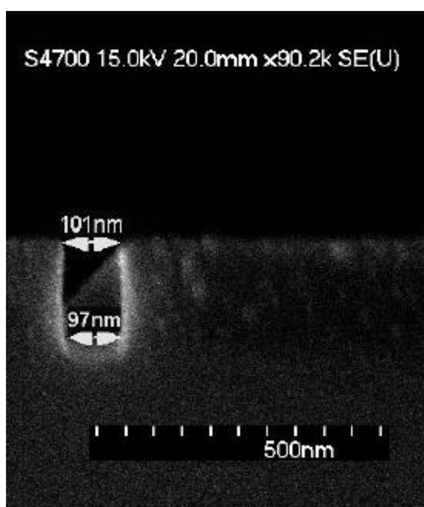

Fig. 1 Cross-section image of cap-recess E-beam lithography.

3. 結果と考察(Results and Discussion)

Fig. 2 and 3 show DC characteristics of the HfO_2 InAs i QW-MOSFET. The results show AlN passivation layer can enhance interface quality and reduce Dit. The AlN passivation layer and NH_3/N_2 PRP treatments enhances the maximum current by 30% as shown in Fig. 2 and enhances Gm,max by 41% as show in Fig. 3. Subthreshold behavior is shown in Fig. 4. It proved that inserting an AlN layer and PRP treatment can increase gate controllability and S.S is improved from 120 mV/dec. to 90mV/dec. by using NH_3/N_2 gases. PRP treatment can not only smooth the interface between HfO_2 and InAs but also improve high-k quality by passivating the traps/defects inside the oxide.

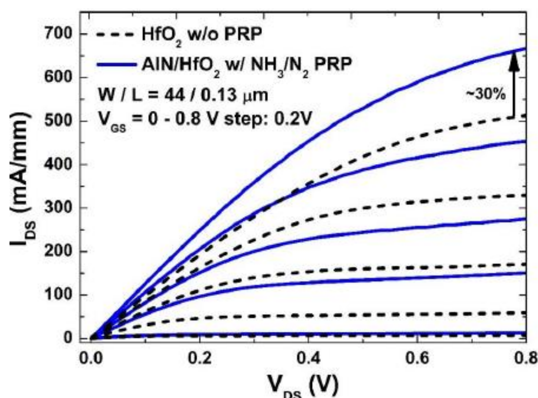

Fig 2 I_{DS} versus V_{DS} of HfO_2 InAs Quantum Well MOSFETs.

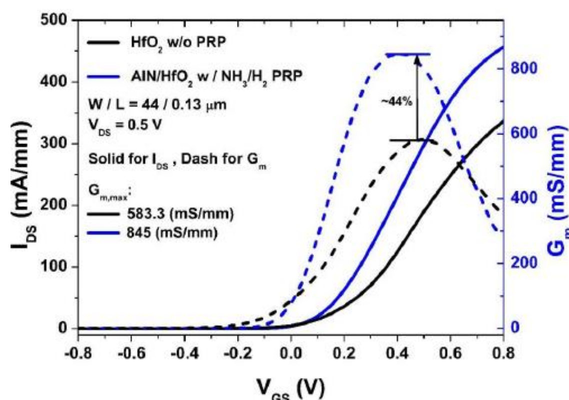

Fig 3 I_{DS}(solid line) and transconductance Gm(dash line) against V_{GS} of HfO_2 InAs QW-MOSFET.

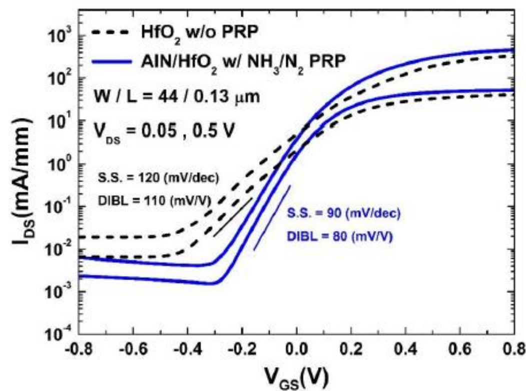

Fig 4 I_{DS} versus V_{GS} subthreshold swing characteristics of HfO_2 InAs QW-MOSFET

4. その他・特記事項（Others）

共同研究者等（Coauthor）：

Y. Miyamoto, Tokyo Tech
Guan-Yu Lin, NCTU
Yueh-Chin Lin, NCTU

5. 論文・学会発表（Publication/Presentation）

Faiz Aizad Fatah, Yueh-Chin Lin, Ren-Xuan Liu, Kai-Chun Yang, Tai-We Lin, Heng-Tung Hsu, Jung-Hsiang Yang, **Yasuyuki Miyamoto**, Hiroshi Iwai, Chenming Calvin HuSayeef SalahuddinEdward Yi Chang, “A 60-nm-thick enhancement mode $In_{0.65}Ga_{0.35}As$/InAs/$In_{0.65}Ga_{0.35}As$ high-electron-mobility transistor fabricated using Au/Pt/Ti non-annealed ohmic technology for low-power logic applications,” Applied Physics Express 9, 026502 (2016)

6. 関連特許（Patent）

None