

課題番号 : F-15-IT-0004
 利用形態 : 共同研究
 利用課題名(日本語) :
 Program Title (English) : 90-nm EBL for manufacturable gate recess etching
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1. 概要(Summary)

MHEMTs with 90-nm gates on InGaAs channel were fabricated. The EBL process was purposely designed with a much smaller design width. This gives ample room for a uniform recess etching across 4" wafers in a manual and over-etching environment.

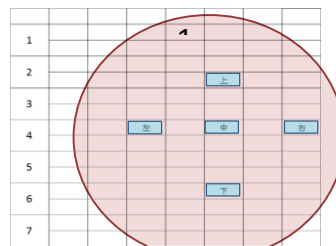


Fig.1 5 measurement locations on wafers

2. 実験(Experimental)

【利用した主な装置】

Electron beam exposure system, Electron-Beam Lithography Software

【実験方法】

A design-width of 50-nm for the gates was implemented at EBL writing, and fine gates exposures were done on the e-beam direct writer JBX-6300 at Tokyo Tech. The rest of fabrication steps followed typical HEMT processes. PCM measurements on $0.09 \times 20 \mu\text{m}^2$ devices at 5 locations on 4" wafers (Fig.1) represent the uniformity across wafers.

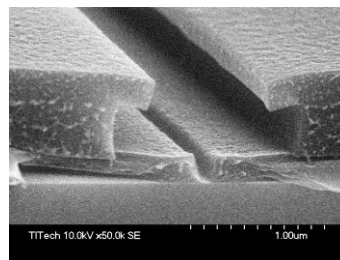


Fig.2 90nm gate EBL by 50nm design-width

3. 結果と考察(Results and Discussion)

Fig.2 is the SEM micrograph of the 90nm gate EBL done by the 50nm design-width process. After completing the gate metallization, DC tests were performed on the PCM devices at 5 locations shown in Fig.1. The (I_{dss} mA/mm, G_m mS/mm) results were (235, 462), (409, 532), (459, 610), (339, 449), and (438, 599). This may suggest that 3/5 or 60% of total area showed reasonably uniform, (i.e., within 10%) $I_{\text{dss}} \sim 435$ mA/mm and $G_m \sim 580$ mS/mm measured at $V_{\text{ds}} = 0.5$ V. The typical $I_{\text{d}}-V_{\text{d}}$ and $G_m(I_{\text{d}}) - V_{\text{g}}$ curves are shown in Fig.3.

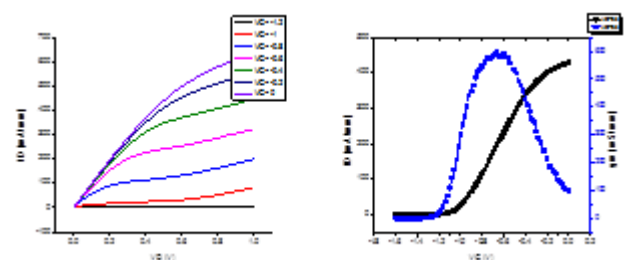


Fig.3 Typical electrical characteristics

4. その他・特記事項(Others)

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5. 論文・学会発表(Publication/Presentation)

None

6. 関連特許(Patent)

None