課題番号　　:F-15-IT-0001
利用形態　　:共同研究
利用課題名（日本語）　:
Program Title (English)　:Study of the T-shaped Gate Head Dimension Influence for 90nm InAs HEMTs on InP Substrate Using E-beam Lithography
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1. 概要（Summary）

In this study, the 90 nm T-shaped InAs HEMTs have been successfully fabricated for high frequency application through two-time exposure of E-beam lithography and low temperature E-beam photoresists development, and the mechanism and the challenges of E-beam lithography will be discussed. Finally, it is demonstrate that the 90nm InAs HEMTs has high speed, high transconductance property.

2. 実験（Experimental）

【利用した主な装置】

electron beam exposure system, Electron-Beam Lithography Software

【実験方法】

The device fabrication process includes mesa etching, Ohmic contact formation, silicon nitride passivation and gate formation. For the gate formation, three photoresists consisting of diluted GL2000 (1:1)/PMGI/GL2000 (180nm/600nm/250nm) from the bottom layer to the top layer were applied on to device open area. After coating, we need soft bake at the temperature of 190^{0}C in 150 seconds layer by layer. Then, the device first exposure (70uC/cm^2) will be executed determining the gate head width. Then, develop first layer-diluted GL2000 (ZED-N50) for 90 minutes and second layer – PMGI (TMAH) for 30 seconds to form a shape similar to a triangle helping to lift off after gate metal deposition. After top two layers' development, second E-beam lithography (900uC/cm2) was applied to determine the critical dimension of the T-shaped gate. In order to enhance the resolution and control ability to the critical dimension, a low temperature development at the temperature of 4^{0}C was used. The result observed under scanning electron microscope (SEM) as shown in Fig. 1.

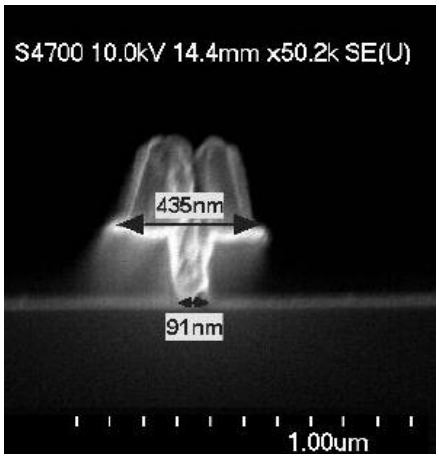

Fig. 1 Cross-sectional SEM images of 90nm T-shaped gate with 400nm gate head width.

3. 結果と考察(Results and Discussion)

Fig. 2 and Fig. 3 show the DC characteristics of the devices with 400 nm gate head lengths. It exhibited drain-source current (I_{DS}) of 405.5 mA/mm when the device is bias at drain voltage (V_{DS}) = 0.5V and gate-source voltage (VGS) = 0.5V as shown in Fig. 2. The maximum transconductance (Gm,max) is 940 mS/mm for the 400 nm gate head width as shown in Fig 3. The S-parameter of the 90nm InAs regular channel HEMTs with 400m gate head width were measured using Agilent E7350A 110GHz S parameter system. A f_T of 70 GHz and fmax of 110 GHz with the gate head width of 400nm was obtained for the devices biases at V_{DS}= 0.5 V and VGS= -0.35 V.

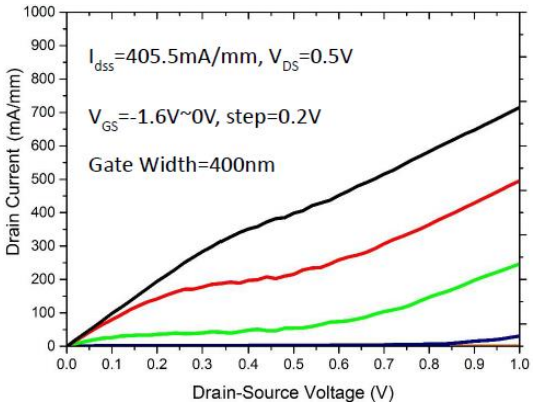

Fig 2 Drain-source current versus drain-source voltage curves for 400nm gate head width InAs HEMTs.

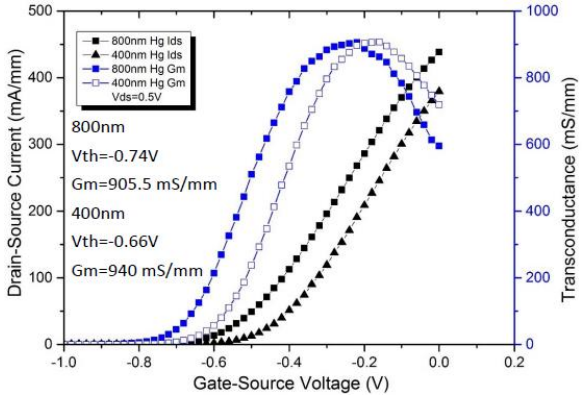

Fig 3 Transconductance versus gate-source voltage at various drain voltages of the InAs HEMTs

4. その他・特記事項（Others）

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5. 論文・学会発表（Publication/Presentation）

Faiz Aizad Fatah, Yueh-Chin Lin, Tsung-Yun Lee, Kai-Chun Yang, Ren-Xuan Liu, Jing-Ray Chan, Heng-Tung Hsu, **Yasuyuki Miyamoto** and Edward Yi Chang, "Potential of Enhancement Mode $In_{0.65}Ga_{0.35}As/InAs/In_{0.65}Ga_{0.35}As$ HEMTs for Using in High-Speed and Low-Power Logic Applications". Solid State Sci. Technol. 2015 volume 4, issue 12, N157-N159.

6. 関連特許（Patent）

None