

課題番号 : F-14-IT-0050
利用形態 : 共同研究
利用課題名 (日本語) :
Program Title (English) : Study of InGaAs Metamorphic HEMTs for Low Noise Amplifier Applications
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1. 概要 (Summary)

The purpose of this research is to develop high frequency HEMT MMIC on 4" epi wafers for low noise amplifier applications. We found that optimized, uniform, and automatic processes are keys to the success of large size wafer processing.

2. 実験 (Experimental)

A set of stepper masks was made for this experiment. The two-fingered $0.09 \times 20 \mu\text{m}^2$ with L_{SD} of 3 μm HEMT devices are the building blocks of MMIC. Fine gates exposures were obtained by e-beam lithography (JBX-6300 at Tokyo Tech, SEM, and surface profiler).

3. 結果と考察 (Results and Discussion)

The e-beam lithography process itself on 4" wafers has been developed and verified, including e-beam resist coating, exposure, and development time etc. When applied to the real device epi wafers, coupled with de-scum cleaning and recess etching of the gate regions, unexpected problems started to show up. Most areas showed that after initial drop in source-drain current it did not continue to decrease as recess etching continued. After the gate metal was deposited and the transistor passivated, the devices did not behave like normal transistors (see the I_d vs V_d figure). In particular, the curves show that the gate is not able to pinch off the channel current at $V_d = 0$ V. This is consistent with the recess-etching observation that the S-D current not continuing to decrease to some pre-determined low current.

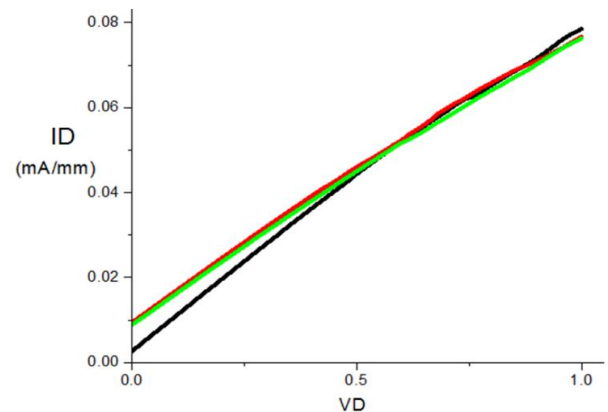


Fig.1 I_d - V_d characteristics

Some corrective actions have taken place. The e-beam exposure dose to the bottom resist will increase. So is the resist development time. All these actions have applied to the most recent wafers. The effectiveness of these changes will be verified later.

4. その他・特記事項 (Others)

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5. 論文・学会発表 (Publication/Presentation)

None

6. 関連特許 (Patent)

None