課題番号　　　　　　　:F-14-IT-0048
利用形態　　　　　　　:共同研究
利用課題名（日本語）　:
Program Title (English)　:Optimization of Gate Recess-etch Current for Device Performance
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1．概要(Summary)

MHEMTs with 90-nm gates on $In_{0.53}Ga_{0.47}As$ channel were fabricated. This research concentrated on gate recess-etch optimization. Because the wafers have no built-in etching stop, finding the accurate relationship of Idss and gm vs. I_{sat} is necessary.

2. 実験(Experimental)

The two-fingered $0.09x20um^2$ devices with InGaAs channel and L_{SD} of 3 um were fabricated following typical HEMT processes, and fine gates exposures were obtained by e-beam lithography (JBX-6300 at Tokyo Tech). The gate recess etching process was then performed to stop at different current levels.

3. 結果と考察(Results and Discussion)

Fig.1 shows the Idss and gm vs. Isat results. We can find out that Isat = 25mA (V=1) gives the highest gm of 598.1 mS/mm. However, decreasing Idss with increasing Isat to 25mA is quite unreasonable. This indicates that more experiment is needed for further verification.

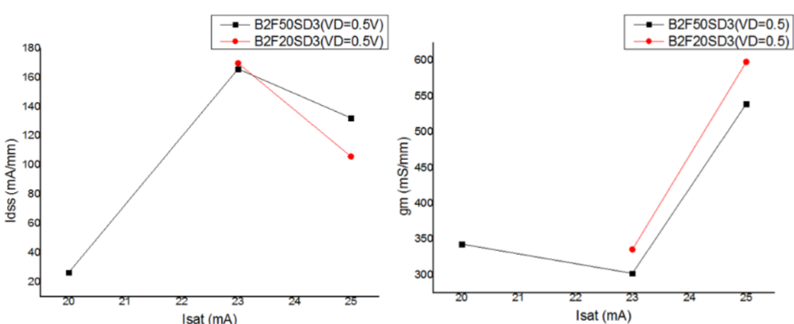

Fig. 1 Idss and gm vs Isat

The device can perform at I_{dss} =105.9 mA/mm and peak g_m = 598.1 mS/mm at V_{DS} = 0.5 V.

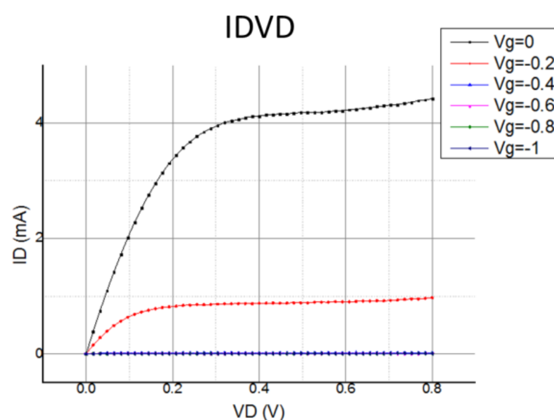

Fig. 2 Output characteristics

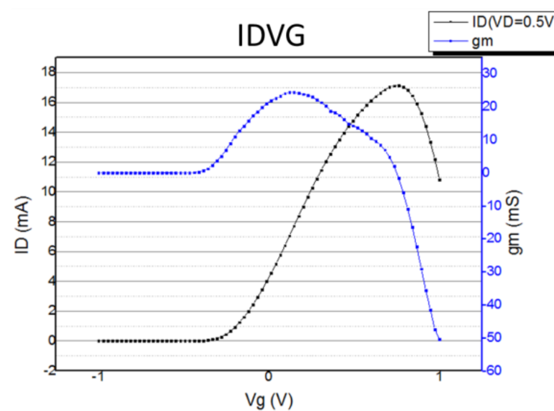

Fig. 3 Transfer characteristics

4. その他・特記事項(Others)

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5. 論文・学会発表(Publication/Presentation)

None

6. 関連特許(Patent)

None