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Program Title (English)	: Study of Tri-Gate $In_{0.6}Ga_{0.4}As$ mHEMTs for Low-Power Logic Applications
利用者名(日本語)	:張翼
Username (English)	:Edward Yi Chang
所属名(日本語)	:国立交通大学 材料工学科,台湾
Affiliation (English)	:Department of Materials Science and Engineering,
	National Chiao Tung University, Taiwan

<u>1. 概要(Summary)</u>

The 150 nm tri-gate $In_{0.6}Ga_{0.4}As$ mHEMTs by 3D structure not only increase the contact area between gate and channel but enhance the gate controllability. The devices with fins display improvement of logic performance at low bias voltage. At V_{DS} of 1.5V, the best sub-threshold swing (SS) of this device is 108mV/dec and I_{ON}/I_{OFF} ratio is 2.1 x 10³. The experiment results show the fin recess process can improve the SS and I_{ON}/I_{OFF} ratio.

<u>2. 実験(Experimental)</u>

The device fabrication process includes mesa etching, ohmic contact formation, annealing, and Si_3N_4 passivation. After that, two electron beam lithography (JEOL JBX-6300SJ) and etching processes are proceeded, including definition of fin recess region and definition of gate recess region. Finally is gate formation and gate metal deposition.

<u>3. 結果と考察(Results and Discussion)</u>

Figure 1 shows the measured current-voltage characteristics of the In_{0.6}Ga_{0.4}As mHEMT with 80 seconds fin recess time. The drain current of device is 378mA/mm and the g_m of devices is nearly 280 mS/mm. Figure 2 exhibits the subthreshold characteristics of the device with 80sec fin recess. The sub-threshold swing (SS) of this device at $V_{DS} = 1$ V is 115 mV/dec. which represents the switch transition of the device is precipitous. Drain Induced Barrier Lowering (DIBL) is calculated to be 333 mV/V at $V_{DS} = 1$ V. The DIBL correlates with an overall insensitivity of V_T to circuit design details and manufacturing variations. The sharp sub-threshold characteristics result in an I_{ON}/I_{OFF} ratio of 1.4 x 10³.



Fig.1 Drain-source current versus drain-source voltage curves of 150nm In_{0.6}Ga_{0.4}As mHEMT with 80sec fin recess



Fig.2 The sub-threshold characteristics of 150nm $In_{0.6}Ga_{0.4}As$ mHEMTs at the V_{DS} of 0.1 and 1V

<u>4. その他・特記事項(Others)</u> 共同研究者等(Coauthor): Y. Miyamoto, Tokyo Tech Jing-Ray Chan, NCTU Yueh-Chin Lin, NCTU

<u>5. 論文·学会発表(Publication/Presentation)</u> None

<u>6. 関連特許(Patent)</u>

None