利用課題番号　：F-13-NM-0003
利用形態　：機器利用
利用課題名（日本語）　：
Program Title（English）　：Alignment mark and TSV formation on Si
利用者名（日本語）　：成 小晋
Username（English）　：Xiaojin Cheng
所属名（日本語）　：独立行政法人 産業技術総合研究所
Affiliation（English）　：National Institute of Advanced Industrial Science and Technology (AIST)

１．概要（Summary）：

This project focuses on developing the 3D IC packaging techniques, which will enable the integration of point-of-care testing for clinical assessment. The main objectives are 1) to develop low-capacitance a Through Silicon Via (TSV) technology with reliable performance by optimizing the fabrication process and materials; 2) to investigate the reliability of the stacked Si interposer/chip after bonding TSVs with Au bumps. The experiments in NIMS are to carry out the lithography, metal deposition and BOSCH process as parts of TSV fabrication procedures. It is finally to serve the evaluation on electrical performance of TSVs in a Si interposer.

２．実験（Experimental）：

【主に利用した装置】
マスクアライナー／Mask Aligner
全自動スパッタ装置／Automatic Sputter
シリコン深堀エッチング装置／Si Deep Etcher
【実験方法】
TSVs were fabricated on 3 inch wafer with a 100 μm thickness. Main procedures are as follows: 1) Alignment marks formation on frontside wafer via Mask aligner (Layer 1). 2)metal Au/Ti deposition in 200 nm/10 nm thickness using Automatic Sputter. 3)Lift-off process. 4)Alignment marks formation on backside wafer via Mask aligner (Layer 1 backside). 5) metal Au/Ti deposition in 200 nm/10 nm thickness using Automatic Sputter. 6)Lift-off process. 7)ZnO deposition using Automatic Sputter. 8)Glass support substrate attchment. 9)Layer 2 aligment with Layer 1 on frontside wafer via Mask aligner for TSV pattern. 10) BOSCH process for TSV formation by Si Deep Etcher.

３．結果と考察（Results and Discussion）：

TSV fabrication has been achieved at the wafer-level. Vias with aspect ratios of 2.5, 4.5, 8.0 and 14.0 were formed on a 100 μm thickness wafer by mean of through silicon etching.

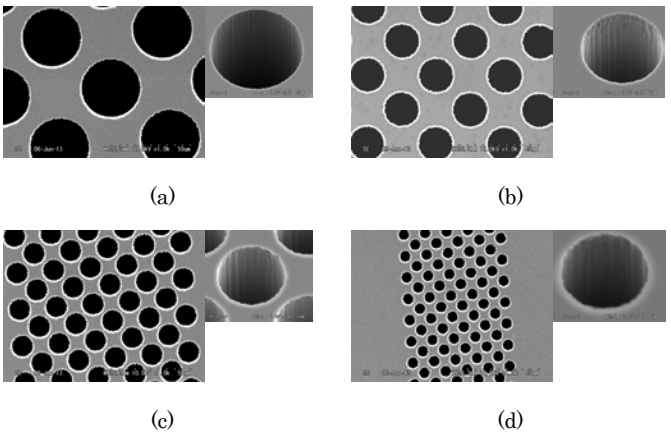

Figure 1 SEM images of TSVs from wafer backside and frontside in zoom-in view (right top corner) with aspect ratio of (a) 2.5; (b) 4.5; (c) 8.0; (d)14.0, respectively.

４．その他・特記事項（Others）：

The other procedures of TSV fabrication process: deposition of insulation layer, Cu electroplating as TSV filler, test pad formation on bothside of wafer will be carried out in AIST. Electrical measurement will then be conducted.

５．論文・学会発表（Publication/Presentation）：

N/A

６．関連特許（Patent）：

N/A