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| 課題番号 | :F-13-IT-0041 |
| 利用形態 | :共同研究 |
| 利用課題名（日本語） | :高速・低電力論理応用の為のエンハンスメントモード InAs HEMTsの研究 |
| Program Title (English) | :Study of Enhancement Mode InAs HEMTs for High-Speed and Low-Power Logic Applications |
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## 1. 概要（Summary）


The enhancement mode 60 nm InAs HEMTs is investigated for high-speed and low-power logic applications. Excellent device performances in low applied voltage that the lower drain induced barrier lowering of 70 mV/V, sub-threshold swing of 67 mV/decade, and higher $I_{ON}/I_{OFF}$ were achieved owing to two-step recess and Pt gate sinking technologies for the device fabrication.


## 2. 実験（Experimental）

The device fabrication process includes mesa etching, Ohmic metal deposition and annealing, silicon nitride passivation and gate formation. Before the formation of T-shaped gate photoresist, a 50 nm silicon nitride thin layer was deposited by plasma enhanced chemical vapor deposition (PECVD) as the support of the following 60nm gate foot. Then, the T-shaped gate photoresist was carried out by using electron beam lithography system (JBX-6300 at Tokyo Tech).

## 3. 結果と考察（Results and Discussion）

Figure 1 shows the drain-source current of 252 mA/mm when device bias at $V_{DS}$ = 0.5 V and $V_{GS}$ = 0.5 V. Figure 2 exhibit s the subthreshold characteristics of the device with different drain biases. Drain Induced Barrier Lowering (DIBL), which measures the change in $V_T$ as a result of a change in $V_{DS}$, is calculated to be 70 mV/V at $V_{DS}$ = 0.5 V. This small DIBL correlates with an overall insensitivity of $V_T$ to circuit design details and manufacturing variations. The sub-threshold slope (SS) of this device at $V_{DS}$ = 0.5 V is 67mV/dec, which represents the switch transition of the device is steep. The sharp sub-threshold characteristics result in an $I_{ON}/I_{OFF}$ ratio of $1.69\times10^4$.

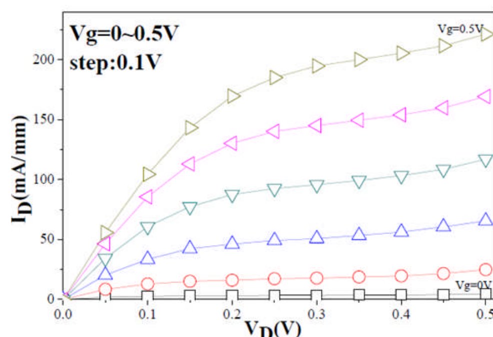


Fig.1 $I_{DS}$ versus $V_{DS}$ curves for the E-mode InAs/$In_{0.65}Ga_{0.35}As$ composite-channel HEMT

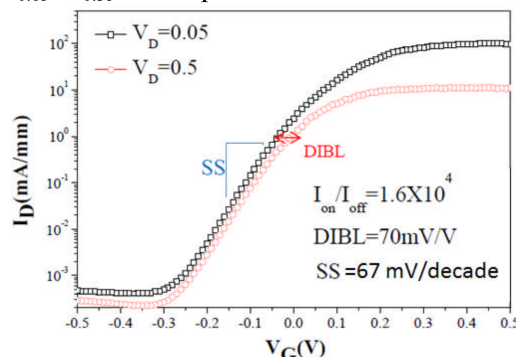


Fig.2 The sub-threshold characteristics (DIBL, SS, $I_{ON}/I_{OFF}$ ratio) of the 60nm enhancement mode InAs HEMTs at the $V_{DS}$ of 0.05 and 0.5V.

## 4. その他・特記事項（Others）

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## 5. 論文・学会発表（Publication/Presentation）

None

## 6. 関連特許（Patent）

None