課題番号 : F-12-TT-0020
支援課題名（日本語） : プラズマを利用しない MEMS 犠牲層 Si エッチング
Program Title（in English） : Plasmaless Si etching for MEMS sacrificial layer removal
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概要（Summary）:

Wet chemistry or chemical dry etching that produces atomic fluorine (F) such as XeF_2 and ClF_3 have been used for the sacrificial layer removal of micro-electro-mechanical system (MEMS). Wet etching techniques require expensive harsh chemical disposal, and chemical dry etching techniques use expensive and/or highly reactive gases such as XeF_2, BrF_3, BrF_5, ClF_3 [Ibbotson et al. J. Appl. Phys. 56 (1984) 2939.]. We have previously reported that single crystal Si (100) can be etched using NO/F_2 gas mixture at the vertical etch rate, E_v, of ~ 5 μm/min utilizing F atoms generated by the reaction of $F_2 + NO \rightarrow FNO + F$ at room temperature [Tajima *et al.* JSAP Spring 17p-A7-14; Fall 13a-F7-4 (2012).]. This E_v was comparable to that by XeF_2. In this study, we evaluated *Ev*, etched profiles, and etched morphology of Si not only in NO/F_2 gases but also in NO_2/F_2 gases while modulating the substrate temperature and the total flow rate, f_{tot}. The MEMS structure fabricated at Toyota Technological Insititute, Nanotechnology Platform Program was used to evaluate the degree of sacrificial layer removal at different etching conditions.

実験（Experimental）:

Two different Si samples were prepared and they were diced into 6 mm × 15 mm in size. One was p-type Si (100) wafer with 100-nm-thick SiO_2 mask with 8 μm × 8 μm square openings, and the other was MEMS structure fabricated by Prof. M. Sasaki group (マスクアライナ装置、レジスト処理装置、洗浄ドラフト一式、ダイシング装置を利用). Ar/NO_x (x = 1 or 2) /F_2 at f_{tot} of 50 to 250 sccm were introduced into the process chamber while maintaining the process pressure at 600 Pa throughout the process time of 300 s.

結果と考察（Results and Discussion）:

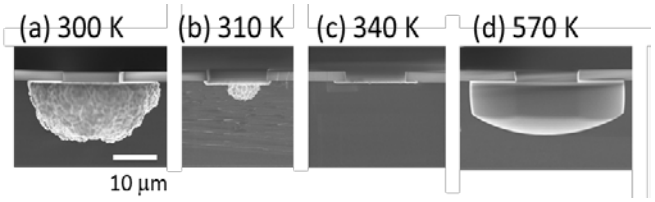

Fig. 1. p-type Si(100) with 10 x 10 μm square SiO_2 mask patterns were etched in the NO/F_2 gas mixture at the substrate temperature *T* at (a) 300 K, (b) 310 K, (c) 340 K, and (d) 570 K.

The etched p-type single crystal Si (100) with SiO_2 hard mask with 10 μm x 10 μm square patterns at substrate temperature in the range of 300 ~ 570 K were shown in Fig. 1. The E_v was ~ 5 μm/min at T = 300 K. The significant reduction in E_v was observed when T increased from 300 K to 340 K. The E_v was increased when T > 340 K and became the E_v at ~2-3 μm/min at 570 K. The orientation dependent etching was achieved at T = 570 K. The MEMS sacrificial layer was successfully removed at T = 300 K and 570 K.

その他・特記事項（Others）：なし

共同研究者等（Coauthor）：林 俊雄

論文・学会発表（Publication/Presentation）:

学会発表 S. Tajima, T. Hayashi, K. Ishikawa, M. Sekine, and M. Hori, The 60th JSAP Spring meeting, 29a-G7-1, Kanagawa Institute of Technology, Japan.

発表論文 S. Tajima, T. Hayashi, K. Ishikawa, M. Sekine, and M. Hori, J. Phys. Chem. C 117 (2013) 5118-5125.

S. Tajima, T. Hayashi, K. Ishikawa, M. Sekine, and M. Hori, J. Phys. Chem. C 117 (2013) 20810-20818.

関連特許（Patent）：特許出願中 3 件